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1	US 20050220242 A1	20051006	19	Locking-status judging circuit for digital PLL circuit	375/376
2	US 20030185330 A1	20031002	12	Phase lock loop and method for coded waveforms	375/376
3	US 20030112915 A1	20030619	17	Lock detector circuit for dejitter phase lock loop (PLL)	375/376
4	US 20020136340 A1	20020926	76	Two-stage multiplier circuit	375/373
5	US 20010046266 A1	20011129	149	Apparatus and method for scdma digital data transmission using orthogonal codes and head end modem with no tracking loops	375/259
6	US 6891881 B2	20050510	160	Method of determining an end of a transmitted frame in a frame-based communications network	375/143
7	US 6701140 B1	20040302	19	Digital receive phase lock loop with cumulative phase error correction and dynamically programmable correction rate	455/260
8	US 6665362 B1	20031216	19	Digital receive phase lock loop with phase-directed sample selection	375/376
9	US RE37751 E	20020618	20	Apparatus and method for transient suppression in synchronous data detection systems	327/100
10	US 6219395 B1	20010417	6	Phase alignment of frames in computer telephony busses	375/371
11	US 6044092 A	20000328	8	Method and apparatus for performing automatic synchronization failure detection in an ATM network	370/516

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15	US 5809096 A	19980915	11	Digital transmission system comprising decision means for changing the synchronization mode	375/375
16	US 5790538 A	19980804	14	System and method for voice Playout in an asynchronous packet network	370/352
17	US 5673004 A	19970930	13	Method and circuit for controlling digital processing phase-locked loop for network synchronization	331/1A
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13	331/18; 370/503	Casper; Paul W. et al.
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17	327/156; 327/159; 331/14; 331/25; 331/DIG. 2; 375/356; 375/357; 375/376	Park; Jung-Hee
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20	US 4459701 A	19840710	16	Process and device for synchronizing at reception digital signals transmitted in packages	375/360
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22	329/311	Pagano; Carmine N. et al.